REMARKS

Claims 1-15 are now pending in the application. Claims 1 and 3-15 are allowed. Claim 2 stands rejected. Applicant has amended Claim 2 to include a control processor that selectively utilizes a delay function in order to change a value of an output means within a predetermined number of cycles of a standard clock, the predetermined number of cycles being configurable by the control processor. The Examiner is respectfully requested to reconsider and withdraw the rejection in view of the amendments and remarks contained herein.

REJECTION UNDER 35 U.S.C. § 102

Claim 2 stands rejected under 35 U.S.C. § 102(b) as being anticipated by Charles et al. (U.S. Pat. No. 5,790,842). This rejection is respectfully traversed.

Referring to Claim 2, Charles et al. do not show, teach, or suggest a control processor that selectively utilizes a delay function in order to change a value of an output means synchronously with a standard clock and within a predetermined number of cycles of the standard clock, the predetermined number of cycles being configurable by the control processor.

Charles et al. teach a set top box processing system that permits simultaneous utilization of two system clocks. The set top box processing system includes an ASIC processor and clock circuitry (col. 8, line 45). The clock circuitry allows elements of the set top box processing system such as a video decoder and an NTSC encoder to communicate with the ASIC processor while using different clocks (col. 18, line 42 and See FIG. 5A). The video decoder and the NTSC encoder operate using a first clock

and the ASIC processor operates using a second clock that is a non-integer multiple of the first clock (col. 20, line 66).

A synchronous phase detector generates an enable signal based on the first and second clocks (col. 19, line 3). The enable signal transitions high when both the first and second clocks transition high simultaneously. The ASIC processor utilizes clock frequency conversion hardware including flip-flops and multiplexers to allow the video decoder and the NTSC encoder to communicate with state-based logic in the ASIC processor (col. 20, line 17). The clock frequency conversion hardware converts the clock frequencies based on the first and second clocks and the enable signal (See FIG. 6A).

The state-based logic does not selectively utilize a delay function in order to change a value that is output by the flip-flop 272 (See FIG. 6A) synchronously with the first clock and within a predetermined number of cycles of the first clock, as required by the claim. The state-based logic is only capable of changing the value that is output by the flip-flop 272 when both the first and second clocks transition high. This occurs every two cycles of the first clock, as admitted by the Examiner. **Second (Final) Office Action, p. 5 (March 14, 2005).**

Also, the number of cycles of the first clock after which the output of the flip-flop is changed is not configurable by the state-based logic, as required by the claim. The state-based logic changes the value that is output by the flip-flop 272 immediately after the value that is input from flip-flop 260 is processed. In other words, Charles et al. do not teach that the state-based logic is capable of remaining in a hold state for a

predetermined number of cycles of the first clock before changing the value at that is output by the flip-flop 272, as taught by Applicant.

Applicant teaches that the control processor may generate the output signal after a predetermined number of cycles of the standard clock. Unlike the clocks in the system taught by Charles et al., the high speed clock is an integer multiple of the standard clock. Therefore, the control processor is capable of generating the output signal synchronous with the standard clock and within any predetermined number of cycles of the standard clock. Additionally, the control processor optionally utilizes a delay function in order to remain in a hold state for a predetermined number of cycles of the standard clock before generating the output signal.

ALLOWABLE SUBJECT MATTER

Applicant acknowledges the allowance of Claims 1 and 3-15 and accordingly thanks the Examiner.

CONCLUSION

It is believed that all of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicant therefore respectfully requests that the Examiner reconsider and withdraw all presently outstanding rejections. It is believed that a full and complete response has been made to the outstanding Office Action, and as such, the present application is in condition for allowance. Thus, prompt and favorable consideration of this amendment is respectfully requested. If the Examiner believes that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at (248) 641-1600.

Respectfully submitted,

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